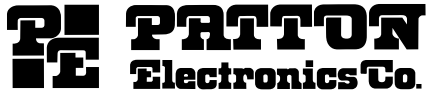


Dos #: 180001UA
Part #: 07M2072-A



INTERFACE CONVERTER, G.703

2072

(CTS IC-G.703)

INSTALLATION AND OPERATIONS MANUAL

January 10, 2000



*An ISO-9001
Certified Company*

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RADIO AND TV INTERFERENCE

The Patton devices generate and use radio frequency energy, and if not installed and used properly—that is, in strict accordance with the manufacturer's instructions—may cause interference to radio and television reception. The Patton devices have been tested and found to comply with the limits for Class A computing devices in accordance with the specifications in Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection from such interference in a commercial installation. However, there is no guarantee that interference will not occur in a particular installation. If the Patton devices do cause interference to radio or television reception, which can be determined by disconnecting the cables, the user is encouraged to try to correct the interference by one or more of the following measures: moving the computing equipment away from the receiver, re-orienting the receiving antenna, and/or plugging the receiving equipment into a different AC outlet (such that the computing equipment and receiver are on different branches).

Canadian EMISSIONS

This digital apparatus does not exceed the Class A limits for noise emissions from a digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la Class A prescrites dans le Règlement sur le brouillage radioélectrique édicté par le ministère des Communications du Canada.

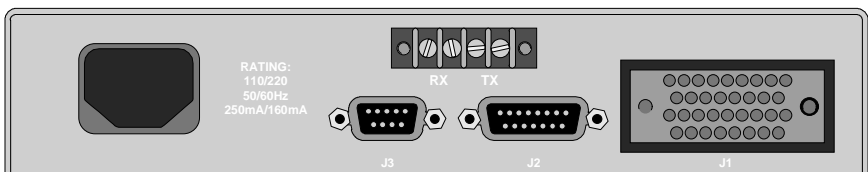
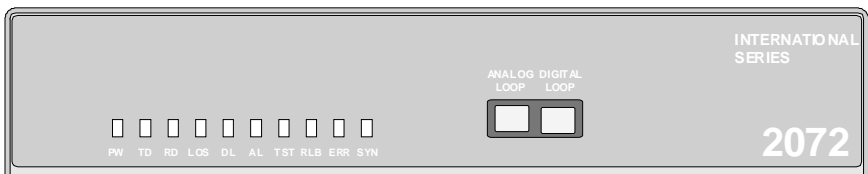
CHAPTER 1 - Operation

The Patton 2072 (CTS IC-G.703) is a CCITT G.703 Co-Directional rate and interface converter. Both CCITT V.35 and CCITT X.21 interfaces are provided for. An M-34 connector for V.35 and a DB-15 connector for X.21 are located on the rear panel. The interface converter operates bi-directionally. DCE / DTE selection of the ports permits interfacing terminals or modems to the G.703 interface converter. This adapter is switch selectable for 48Kbps, 56Kbps or 64Kbps data rates. When configured for 48Kbps or 56Kbps, it will provide an additional asynchronous service channel.

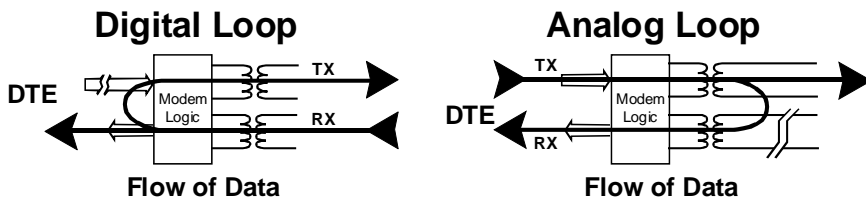
The 2072 (CTS IC-G.703) can be clocked from the recovered clock of the receive pair. Can be provided to the 2072 (CTS IC-G.703) by an attached device externally or be generated by the 2072 (CTS IC-G.703) internally. Elastic buffers are provided to compensate for the phase difference between clocks.

The 2072 (CTS IC-G.703) fully conforms to the G.703 CCITT standard by performing the required "1's density" bit stuffing every 7 bits. Additionally it will pass a control signal from end to end or the 1200 bps asynchronous service channel for enhanced line utilization.

A built in Burst Error Rate Tester (BERT) and both Analog and Digital Loop Back allow the user flexibility in circuit verification and testing. When either Loop Back button indicates **BLACK** (OUT), that loop back is disabled and all signals pass normally through the 2072 (CTS IC-G.703). When either Loop Back button indicates **GREEN** (IN), that loop back is enabled. The 2072 (CTS IC-G.703) implements digital and analog loop back of the data



and clocks. Analog Loop turns the data around at the analog interface to the G.703 interface. When Analog Loop is selected the **AL** LED will illuminate. Digital Loop turns the data around at the V.35 digital interface. When Digital Loop is selected the **DL** LED will illuminate.



If both Loopback buttons indicate **GREEN** (IN) then the unit is in Test mode and the **TST** LED will be illuminated. In this configuration, a BERT pattern is sent to the remote 2072 (CTS IC-G.703) unit. If the remote unit detects the BERT pattern and the remote BERT detect option is enabled, the remote unit will turn on its Remote Digital Loopback, illuminate the **RDL** LED and loop the test pattern back to the sending unit to complete the test loop. If errors are detected at the originating 2072 (CTS IC-G.703) the **ERR** LED is illuminated.

The interface converter is housed in a sturdy aluminum enclosure and has an internal 110/220VAC switch selectable power supply.

The unit has UL, and CSA approvals and can operate on standard power found in most countries.

CHAPTER 2 - SETUP AND INSTALLATION

Installation

Set the switches to match the required configurations based on the diagrams below. The cabling between each device and the interface converter must be terminated with male connectors. J1 is the V.35 interface, J2 is the X.21 interface and J3 is the V.24 low speed asynchronous interface. The 4 position terminal block is for the G.703 line connection. The IEC connector is provided to interface to the power plug required in the country of use. Insure the 110/220VAC switch is set correctly for the line voltage in use prior to applying power to the interface converter.

Selection of DTE/DCE

To connect a terminal type device (DTE) to the 2072 (CTS IC-G.703), connect the Terminal to J1 or J2 and move SW1, SW2, and SW3 to the rear of the unit toward the connectors (**DCE** position).

To connect a Modem type device (DCE) to the 2072 (CTS IC-G.703), connect the Modem to J1 or J2 and move SW1, SW2, and SW3 to the front of the unit away from the connectors (**DTE** position).

Equipment Grounding

JP7 provides grounding interconnection in those systems requiring a connection between Frame Ground and Signal Ground. If signal ground and chassis ground interconnection is desired, install the jumper on JP7.

LED Indicators

The Following LED indicators are provided for diagnostics: Power (PW), Transmit Data (TD), Receive Data (RD), Loss of Signal (LOS), Digital Loopback (DL), Analog Loopback (AL), Test (TST), Remote Loopback (RLB), Error (ERR) and Sync (SYN).

Front Panel Loop Back Buttons

The Digital Loop and Analog Loop buttons are provided to enable and disable the testing and loopback features.

Data Rate (SW5-3,4)

Selection of data rates is provided by switch 5, positions 3 and 4. The following chart summarizes the available:

SW5-3	SW5-4	Rate
ON	ON	48Kbps
OFF	ON	56Kbps
ON	OFF	64Kbps
OFF	OFF	N/A

Control Lead Pass Through / Async Channel (SW5-2)

Selection of the asynchronous service channel or a control lead pass through for 48K and 56Kbps rate selection is provided by SW5 pos 2. If an asynchronous 1200 bps service channel is desired, set SW5-2 to **ON**. If it is desired to pass the RTS when DCE is selected or the DCD when DTE is selected to the remote end, set SW5-2 to **OFF**. The passed control lead will be presented at the far end as an RTS if the IC-G.703 is configured as a DTE or DCD if configured as DCE. This option must match at both ends of the circuit.

Clear to Send (CTS) Control (SW4-6)

Selection of the source for CTS is via Switch 4 pos 6. To force the CTS to active regardless of RTS activity, set SW4-6 to **ON**. If it is desired to allow CTS to follow RTS then set SW4-6 to **OFF**. This circuit is only operational when the 2072 (CTS IC-G.703) is configured as a DCE.

Auto Remote Digital Loop Enable (SW5-5)

To enable automatic Remote Digital Loopback when upon detection of the BERT test pattern set Switch 5 pos 5 to **ON**. To configure the IC-G.703 unit to ignore the test pattern when received set Switch 5 pos 5 to **OFF**.

Loss of Signal or Control Lead to Carrier Detect (SW5-1)

Selection of the source for Carrier Detect (CD) is via Switch 5 pos 1. If you want the remote units selected control lead to appear on the CD interface signal leads of the local units, set SW5-1 to **ON**. If it is desired to have the Loss Of Signal (LOS) on the CD interface signal leads, then set SW5-1 to **OFF**.

MARK Polarity (JP5, JP6)

JP5 and JP6 select the polarity of the G.703 signal when the X.21 or V.35 signal is in a MARK condition. If you require MARK to be a **ZERO** on the G.703 interface, place the header for both JP5 & JP6 on pins 1 & 2.

Looking from the front of the unit this is on the right two pins of both jumpers. If you require MARK to be a **ONE** on the G.703 interface, place the header for both JP5 & JP6 on pins 2 & 3. Looking from the front of the unit this is on the left two pins of both jumpers.

Secondary Async Port CTS Forced or Follows RTS (JP4)

JP4 determines the source of the CTS signal on J3, the asynchronous service port. To force the CTS to constant active, install the header on JP4 pins 2 & 3. For CTS to follow RTS install the header on JP4 pins 1 & 2.

Clocking Modes (SW4-1,2,3,4,5)

Clocking mode selection is provided by Switch 4, positions 1 through 5.

Only one switch position should be set to OFF at any time.

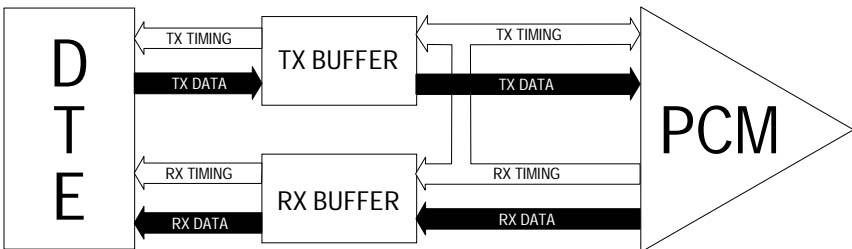
Selecting more than one mode may result in erratic operation of the 2072 (CTSIC-G.703).

The G.703 Co-directional interface specification requires that the Data and Clock will be provided by the same source. The 2072 (CTS IC-G.703) will provide a clock for the data it sends to the central office PCM link. The Central Office provides the clock for the data coming from the Central Office on the PCM link to the 2072 (CTS IC-G.703). This arrangement is fixed in the hardware and cannot be modified.

Clocking on the V.35 and X.21 interface however is very flexible and can be configured to meet any need the user has. The follow descriptions along with the diagrams explain all of the possible clocking modes available to chose from.

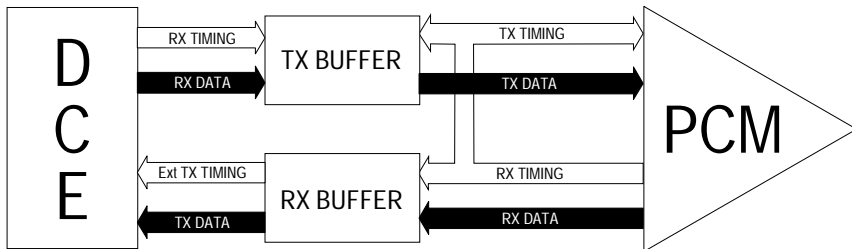
Mode 1 (SW4-1 **OFF**, 2, 3, 4, 5 **ON**)

The 2072 (CTS IC-G.703) provides both receive and transmit clock to a DTE device connected on the V.35 or X.21 interface. The receive clock provided on the PCM channel is used to generate all outgoing clocking. Data passes through both the TX BUFFER and the RX BUFFER using the PCM RX TIMING for both input and output clocks.

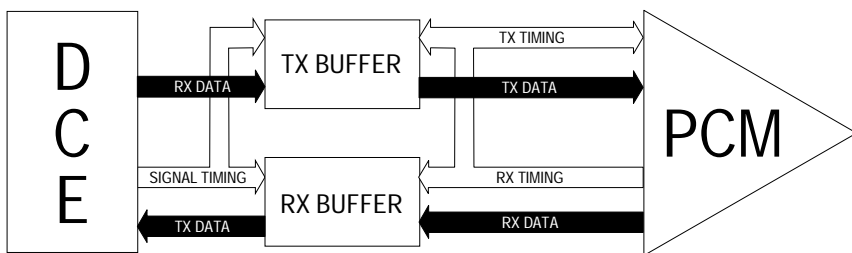


Mode 2 (SW4-2 OFF 1, 3, 4, 5 ON)

The 2072 (CTS IC-G.703) gets its receive clock from a DCE device and gives an external transmit clock to the DCE device connected on the V.35 interface. The receive clock provided on the PCM channel is used to generate all outgoing clocking. Data passes through the RX BUFFER using the RX TIMING for both input and output clocks. Data passes through the TX BUFFER using the DCE TX TIMING for the input clock and PCM RX TIMING for the output clock. This mode is not available for X.21.

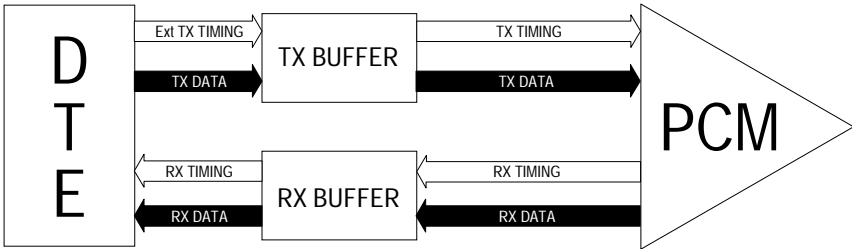
**Mode 3 (SW4-3 OFF 1, 2, 4, 5 ON) X.21 ONLY**

The 2072 (CTS IC-G.703) gets the Signal Timing from the X.21 DCE device connected on the DB-15 interface. The receive clock provided by the PCM channel is used to generate transmit clock for data going to the PCM interface. Data passes through the RX BUFFER using the PCM RX TIMING for the input clock and Signal Timing from the X.21 interface for the output clock. Data passes through the TX BUFFER using the Signal Timing from the X.21 interface for the input clock and PCM TX TIMING for the output clock.

**Mode 4 (SW4-4 OFF 1, 2, 3, 5 ON)**

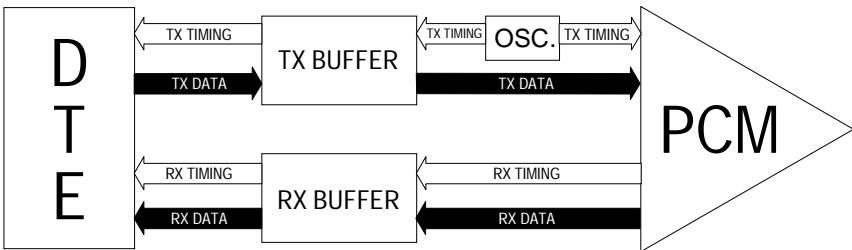
The 2072 (CTS IC-G.703) gets an external transmit clock from the DTE device and gives a receive clock to the DTE device connected on the V.35 interface. The receive clock provided on the PCM channel is used to

generate the receive clock provided to the V.35 interface. The external transmit clock provided on the V.35 interface is used to generate the transmit clock provided to the PCM channel. This mode is not available for X.21.



Mode 5 (SW4-5 **OFF** 1, 2, 3, 4 **ON**)

The 2072 (CTS IC-G.703) gives both the receive and transmit clock to the DTE connected on the V.35 interface. The receive clock provided on the PCM channel is used to generate the receive clock provided to the V.35 interface. An internal time base is used to generate all transmit clocks. This mode is not available for X.21.



Line Terminal Block

The terminal block on the rear panel of the 2072 (CTS IC-G.703) is used to connect to the G.703 PCM system. The input from the G.703 system connect to the terminals labeled RX. The output from the 2072 (CTS IC-G.703) to the G.703 system come from the terminals labeled TX. Both input and output are transformer coupled and are not polarity sensitive.

Factory Test Straps

The Factory Test Straps JP1, JP2 and JP3 must be installed for proper operation of the interface converter.

APPENDIX

TECHNICAL SPECIFICATIONS

Applications

V.35 or X.21 to G.703 Co-Directional interface and rate conversion

Capacity

One Channel V.35 or X.21 to G.703

Data Format

Data Coding: Synchronous

Data Rates

48Kbps, 56Kbps and 64Kbps

Electrical Interface

V.35 or X.21 and G.703

V.35 Physical Interface

V.35 on a Female M-34 Connector

X.21 Physical Interface

X.21 on a Female DB-15 Connector

G.703 Physical Interface

G.703 Co-Directional Interface on a 4 position Terminal Block

Enclosure

Metal: Aluminum

Approvals

CE Pending

Front Panel

Indicators: Power, TD, RD, LOS, DL, AL, TST, RLB, ERR, SYN

Switches: Loop Back

Power Requirements

100-120/200-240VAC, 50 to 60Hz, 0.25/0.16A, Switch Selectable

Environmental

Oper Temp: 32° to 122°F (0° to 50°C)

Rel Humidity: ... Up to 90% non-condensing

Altitude: 0 to 10,000 feet

Dimensions

Height: 1.75 inches (4.44 cm)

Width: 8.90 inches (22.60 cm)

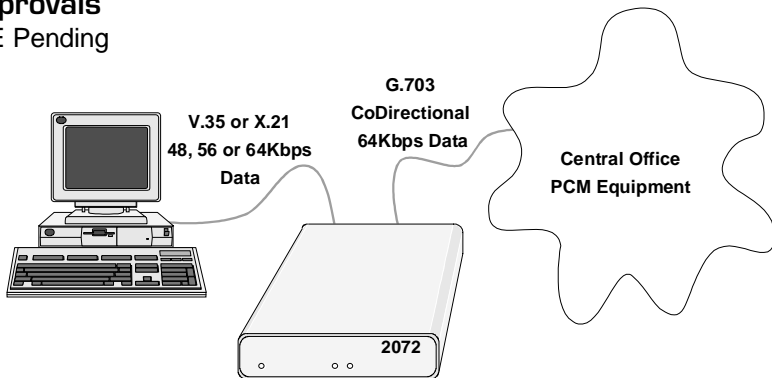
Length: ... 10.00 inches (25.40 cm)

Weight

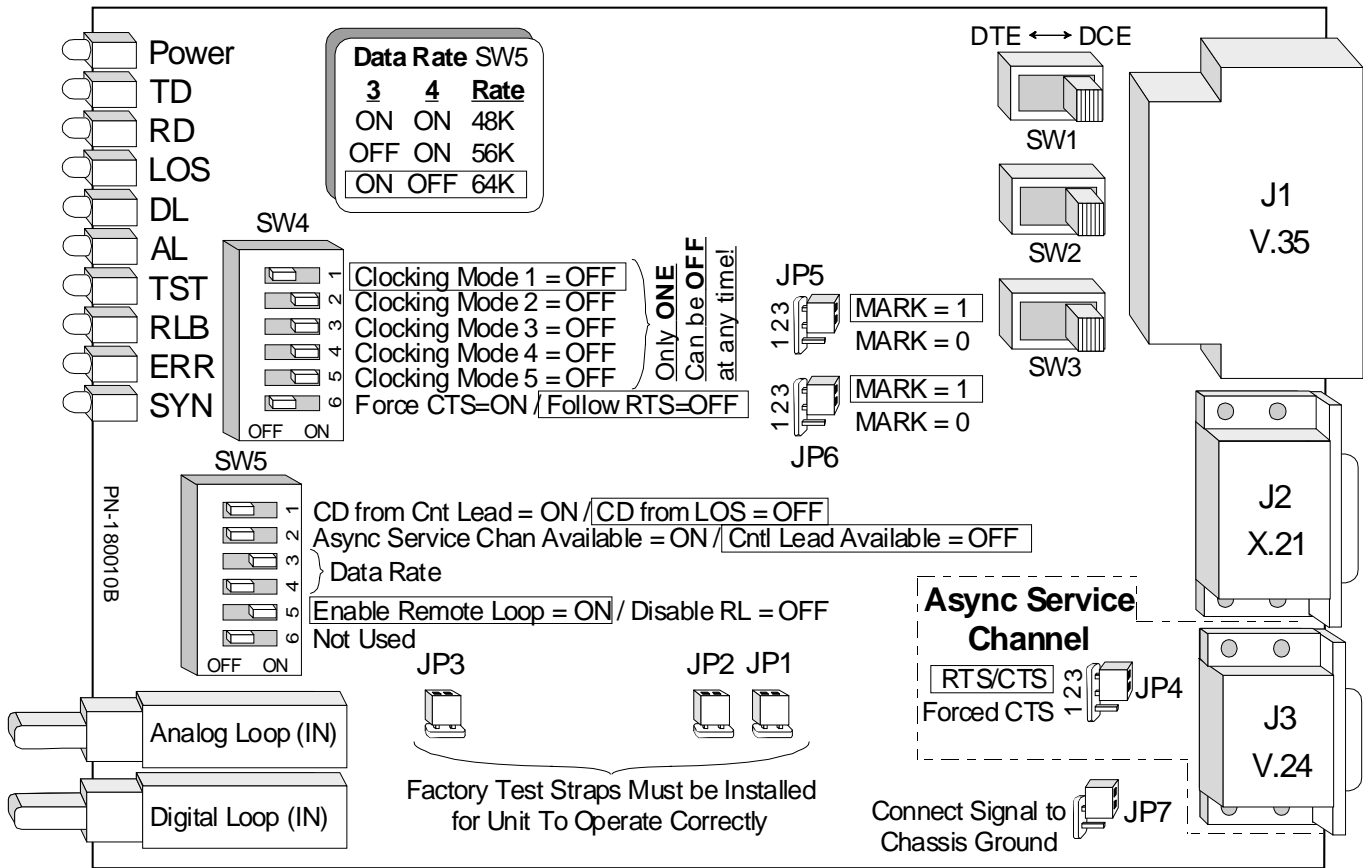
2.25 lbs (1.02 Kg)

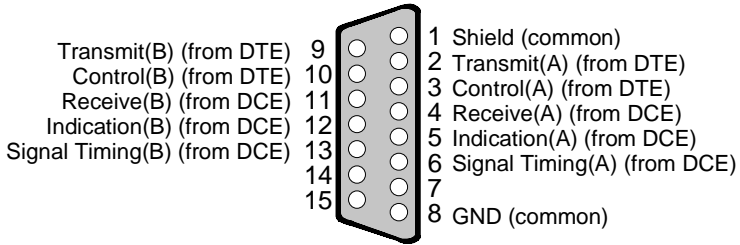
Warranty

Two Years, Return to Factory

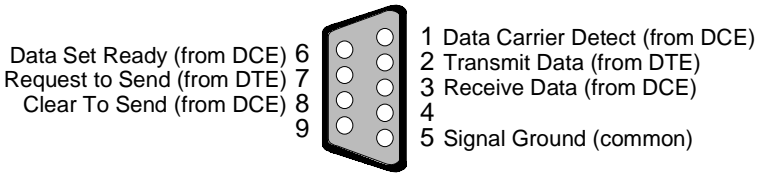


Typical Application

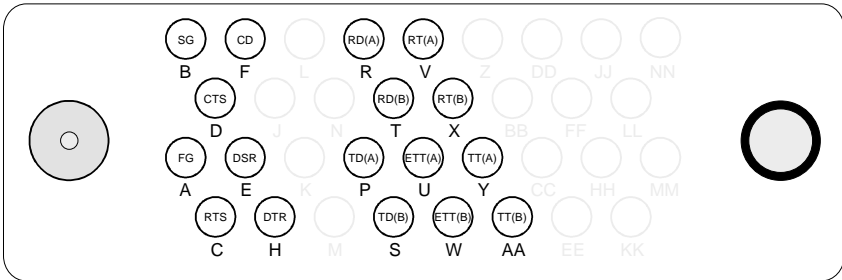




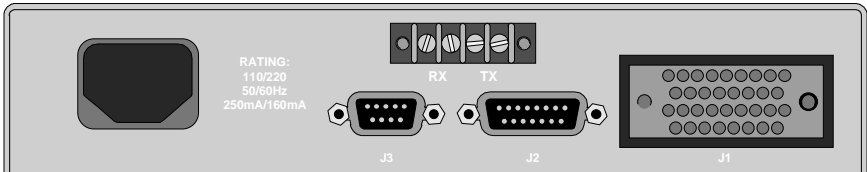
X.21 Interface Pins Supported



V.24 Asynchronous Interface Pins Supported



V.35 Interface Pins Supported



Rear Panel



7622 Rickenbacker Drive
Gaithersburg, MD 20879

Sales: 301 975-1000 Support: 301 975-1007
Web Address: <http://www.patton.com>