Application Note

Using the Model 2066RC X.21 to V.35 Interface Converter At High Data Rates

Introduction

This application note highlights the effects of signal propagation delay and the difficulties that can be encountered when operating the X.21 interface at high data rates (higher than one Mbps). A typical application where the Model 2066RC is used to interface an X.21 DCE with a V.35 DTE will be examined. At data rates above one megabit-per-second, signal delays due to interconnecting cables and the interface converter circuitry become significant and cannot be ignored.

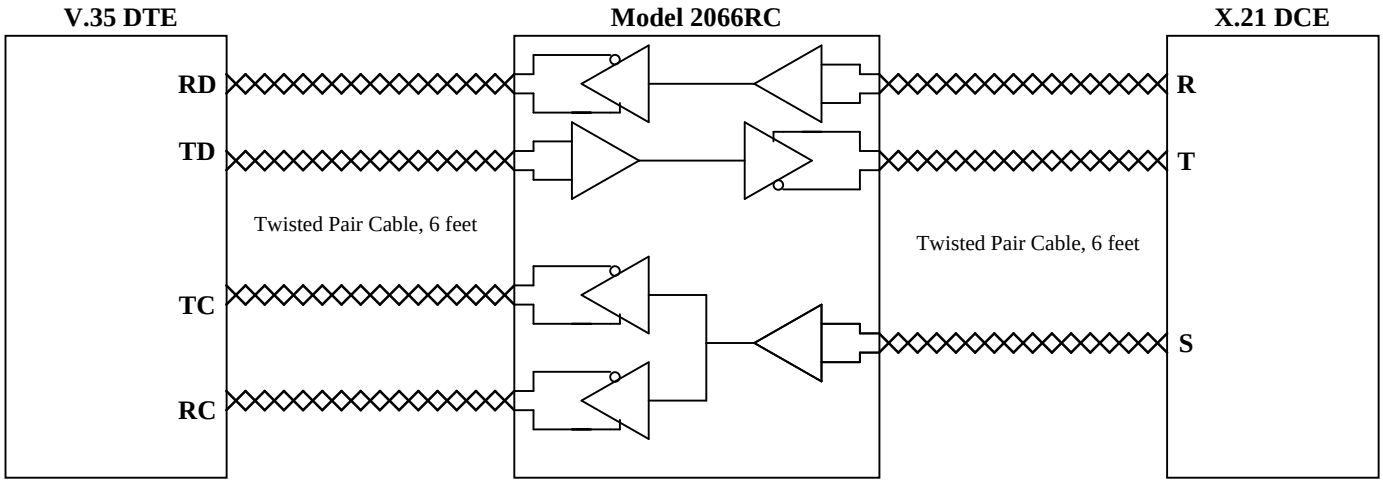

Figure One
X.21 DCE to V.35 DTE Interface Conversion

A Typical 2066RC Application

Figure one shows a typical application for the Model 2066RC. In this example, the Model 2066RC is used to perform the electrical and physical conversions between an X.21 DCE and a V.35 DTE at a data rate of **2.048 Mbps**. For simplicity, only the high speed data and clock signals are shown in the diagram. Appropriate control signals are also converted and passed through the Model 2066RC, as required. Both X.21 and V.35 interfaces employ two-wire, balanced differential signaling for data and clock signals. The two wires that comprise each differential signal will be referred to as the "A" line and the "B" line. The nominal differential voltage at the X.21 interface is between 2 volts and 4 volts. The V.35 differential voltage is specified to be 0.55 volts, ±20%.

In the above example, the X.21 and V.35 devices are connected to the Model 2066RC by two 6-foot twisted pair cable assemblies. The system clock, **S**, is supplied by the X.21 DCE and originates at point "S". The **S** clock is converted to V.35 voltage levels and is then sent to the receive clock (RC) and transmit clock (TC) inputs of the V.35 DTE. The V.35 DTE uses the receive clock to receive (sample) data and uses the transmit clock to send data. The X.21 DCE uses only one clock, the **S** clock, to send and receive data. Both interfaces send data on the rising clock edges (Line A>Line B of the signal pair) and sample data on the falling clock edges (Line B>Line A of the signal pair).

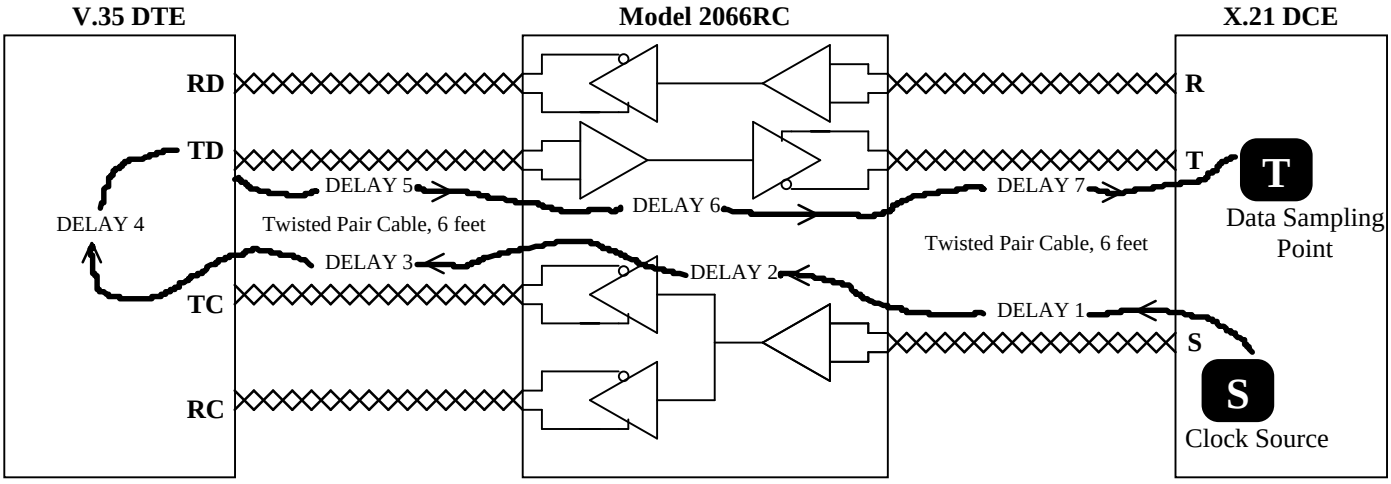

Figure 2
Important Propagation Delays

Figure 2 shows the signal path where propagation delays can be especially harmful to overall system performance. In the example shown above, the system clock, **S**, originates at the X.21 DCE. This clock is used by the X.21 DCE to transmit data (from port **R**) and to receive data (at port **T**). The **S** clock is converted by the 2066RC and is then sent to the V.35 DTE's Transmit Clock and Receive Clock ports. The V.35 DTE uses the Transmit Clock (**TC**) to send data to the X.21 DCE.

At a frequency of 2.048 MHz, one clock period is approximately 488 nanoseconds. If the system shown in Figure 2 were an ideal system, i.e. one with no delays, the data transition at point T would occur exactly on the rising edge of the **S** clock, as shown in Figure 3 below. Additionally, the data sampling point, indicated by the dashed lines, would occur at exactly 50% of the data bit. In a theoretically ideal system running at 2.048 Mbps, the data sampling point would be:

$$\frac{\text{(½ clock period) - (system delay)}}{\text{(clock period)}} = \frac{\text{244ns - 0ns}}{\text{488ns}} = \textbf{50\% into data bit}$$

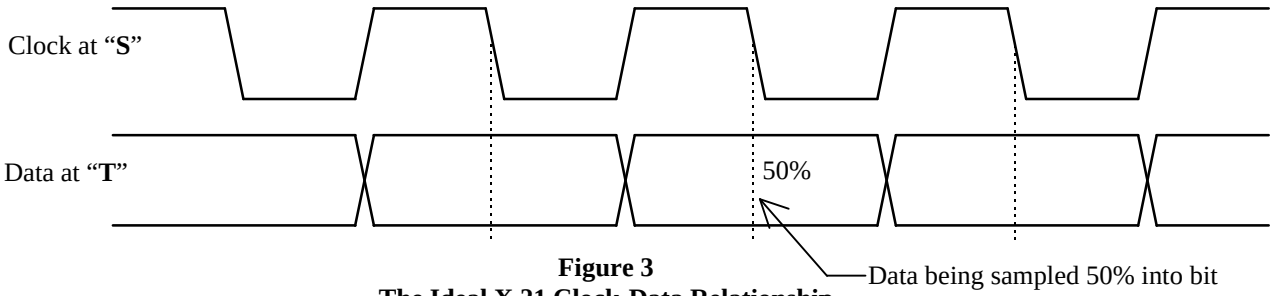

Figure 3
The Ideal X.21 Clock-Data Relationship

Unfortunately, no system is ideal. All components of a data transmission system will introduce some amount of delay into the signal path. As system clock rates increase, the delays shown in the highlighted path may be significant enough to cause data errors at the X.21 DCE equipment (point "T"). In the above application, there are a total of seven delays between a rising edge of the **S** clock, at point "S", and the actual data transition, at point "T". Figure 4 shows an actual S-clock /T-data relationship that was observed at the X.21 DCE device with the system running at a data rate of **2.048 Mbps**. The seven individual delays were measured and are listed below:

Delay 1 - 12 ns - 6 feet of twisted pair cable
Delay 2 - 31 ns - 2066RC conversion circuitry
Delay 3 - 12 ns - 6 feet of twisted pair cable
Delay 4 -108 ns - V.35 DTE terminal delay (rising edge of TC to TD data transition)
Delay 5 - 12 ns - 6 feet of twisted pair cable
Delay 6 - 28 ns - 2066RC conversion circuitry
Delay 7 - 12 ns - 6 feet of twisted pair cable
Total path delay - **215 ns** - (rising edge of **S** clock at "S" to data transition a "T")

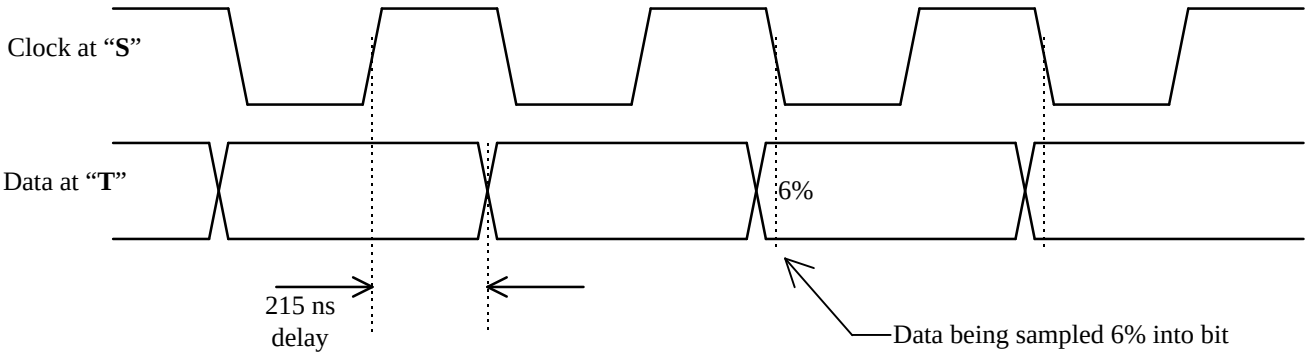

Figure 4
Clock And Data Relationship of Actual System

In this real system, the inherent signal delays cause a shift in the data sampling point. Instead of the ideal sampling point of 50% into the data bit, the 215 nanosecond path delay causes the data to be sampled at only 6% into the data bit.

$$\frac{\text{(½ clock period) - (system delay)}}{\text{(clock period)}} = \frac{\text{244ns - 215ns}}{\text{488ns}} = \textbf{6\% into data bit}$$

As can be seen in Figure 4, the 215 nanosecond delay puts the data sampling point at the X.21 DCE extremely close to the data transitions. This is an undesirable situation and could cause data errors at the X.21 interface.

Preventing Errors at High Data Rates

When using the Model 2066RC in high speed applications, special techniques may need to be employed in order to compensate for inherent system propagation delays. Bit errors will occur when system delays cause data transitions to occur at or near the falling edge of the **S** clock at the X.21 DCE. In the above example, the 215 nanosecond system delay puts the X.21 data sampling point at only 6% of the data bit. This places the data sampling point very near the data transition points. To prevent data errors in this situation, the data transition point at the X.21 DCE (point "T") must be shifted in time (moved closer to the rising edge of the **S** clock).

The simplest method of reducing the effects of system delays is to reduce the data rate, i.e. clock speed. Although this method will not actually reduce the delays of the system, it will lessen their impact by increasing the ratio between the system delays and the period of the system clock, **S**.

If reducing the data rate is not feasible, another method of altering the X.21 **S**-clock/**T**-data relationship must be used. Since the delays of the 2066RC and the data transmission equipment are fixed and cannot be changed, a practical way of moving the data transitions away from the sampling point is to adjust the length of the connecting cables. The propagation delay of the cables is proportional to their length. By increasing or decreasing the length of the connecting cables, the total system delay can be adjusted, as needed

Finally, if the data transitions at the **T** port of the X.21 DCE are falling very near the falling edges of the **S** clock (due to signal delays), simply inverting the Transmit Clock (**TC**) at the V.35 DTE will restore the proper clock-data relationship at the X.21 interface (refer to Figure 3). If the DTE equipment does not provide this clock inversion feature, the Transmit Clock signal may be inverted by physically swapping the connections of the Transmit Clock twisted pair lines at the V.35 interface.